Marked-Up Version Showing Changes Made:

1. (Amended) A shared memory processor-to-processor mailbox between at least two processors, comprising:

a shared memory accessible by a first processor and a second processor, said shared memory including a first mailbox portion to pass data from said first processor to said second processor, and a second mailbox portion to pass data from said second processor to said first processor, said first mailbox portion and said second mailbox portion being defined at least in part over common memory;

said first mailbox portion starting at a low physical address end of said shared memory, and addressably filling upward through to [toward] a highest physical address of said [shared] common memory;

said second mailbox portion starting at said high physical address end of said shared memory, and addressably filling downward through to [toward] said lowest physical address of said [shared] common memory; and

said first processor having write access to said first mailbox portion and not to said second mailbox portion.

8. (Amended) A method of utilizing a shared memory as a mailbox between two processors, comprising:

providing a contiguous block of shared memory;

allocating first direction messages passed from a first processor to a second processor to a first physical address end of said shared memory;

allocating second direction messages passed from said second processor to said first processor to a second physical address end of said shared memory opposite said first physical address end;

allowing said first direction messages to utilize a dynamically allocated shared central portion of said shared memory addressably filling through to [growing toward] said second physical address end; and

allowing said second direction messages to utilize said dynamically allocated shared central portion of said shared memory addressably filling through to [growing toward] said first physical address end.

13. (Amended) Apparatus for utilizing a shared memory as a mailbox between two processors, comprising:

shared memory means for providing a contiguous block of shared memory;

means for allocating first direction messages passed from a first processor to a second processor to a first physical address end of said shared memory;

means for allocating second direction messages passed from said second processor to said first processor to a second physical address end of said shared memory opposite said first physical address end;

means for allowing said first direction messages to utilize a dynamically allocated shared central portion of said shared memory addressably filling through to [growing toward] said second physical address end; and

means for allowing said second direction messages to utilize said dynamically allocated shared central portion of said shared memory addressably filling through to [growing toward] said first physical address end.

REMARKS

Claims 1-17 remain pending in the application.

No new issues are raised, nor is further search required as a result of the amendments made herein. The amendments merely define more clearly the distinctions of the present invention over the prior art of record. It is therefore respectfully requested that the Amendment be entered.

Claims 1-17 over Frampton, Perets and Feemster

In the Office Action, claims 1-17 were rejected under 35 U.S.C. §103(a) as allegedly being anticipated by U.S. Pat. No. 5,802,351 to Frampton ("Frampton") in view of U.S. Pat. No. 5,537,576 to Perets et al. ("Perets") and further in view of Feemster et al. ("Feemster"). The Applicants respectfully traverse the rejection.

Claims 1-7 recite first and second mailbox portions defined at least in part over **common** memory, the first mailbox addressably filling upward through to a **highest** physical address of the common memory, and the second mailbox addressably filling downward through to a **lowest** physical address of the common memory. Claims 8-17 recite a **contiguous** block of **shared** memory, a first mailbox addressably filling upward through to a **highest** physical address of the **common** memory, and a second mailbox addressably filling downward through to a **lowest** physical address of the **common** memory.

It is respectfully submitted that the need to combine as many as THREE references to find the elements of the claims of the present invention is an indication of NON-obviousness of the same.

With respect to the three cited references, Frampton teaches a data interface wherein a dual port memory forms nothing more than a conventional buffer by filling up from the bottom to the top. This arrangement is quite conventional. Even the Examiner admits that Frampton fails to teach filling downward toward a low physical address. (Office Action at 2)

The Examiner cites Perets to allegedly cure this first deficiency. In particular, the Examiner cites Perets, col. 6, lines 32-41; and col. 8, lines 40-52, as allegedly teaching "filling downward toward a low physical address."

To more clearly emphasize an important element of the present invention, claims 1-17 are amended herein to recite "filling downward through to a **lowest** physical address of **common** memory defining a first and second mailbox.

Perets teaches **expandable** memory for a digital signal processor. According to Perets, memory BANKS may be ADDED, e.g., in blocks of 64K, to fill in an otherwise EMPTY addressable section between upper and lower blocks.

The Examiner responds in the Office Action at page 5 by interpreting the dashed lines in Fig. 2 as "an indication that memory bank 14 fills towards the bottom address." This is NOT what the dashed lines in Fig. 2 represent. Perets even DEFINES what those dashed lines represent: "A bottom address of the first memory bank 14 and a top address of the second memory bank 15 are each marked as dashed lines 36 and 37 respectively." (Perets, col. 6, lines 6-9) Perets clearly and explicitly defines the dashed lines 36, 37 as merely representing a bottom address and a top address.

It is improper for the Examiner to re-define the meaning of the dashed lines in Perets, particularly in light of the explicit definition of their meaning.

The Examiner alleges that the Applicants fail to specifically argue why the combination of Framptom and Perets is improper. (Office Action at 5) Framptom teaches a shared memory in the traditional sense, i.e., with a unidirectional buffer filling only upwards. Perets teaches nothing more than **expandable memory** wherein additional memory blocks may be inserted in fixed lengths. The expandable memory may grow from the top, or from the bottom. In any event, Perets does NOT teach a **shared** memory, i.e., shared by two or more accessing devices or processors. A combination of Frampton with Perets, even if proper (which it is not), would arrive at a system with a buffer that nevertheless fills **only from the bottom**. The SIZE of the buffer can be expanded by blocks of memory at the top or bottom per Perets, but the operation of a buffer using that memory would fill only from the bottom. Claims 1-17 all require use of common memory wherein a mailbox fills from the top down.

Perets and Frampton relate to two different types of memory (one to a single port memory, the other to a dual-port memory), and thus are impropertly combined for that reason as well. For instance, expandable memory in general teaches **away** from the present invention, as the present invention relates to the maximization of a given data space (see the title of this application). One of ordinary skill in the art desiring to **maximize** a given space would not have been motivated to look to art for expanding memory such as Perets teaches. Thus, it is respectfully submitted that Perets is improperly combined with Frampton with respect to the present invention.

Moreover, even if the combination was proper (which it is not), the combination STILL would not teach the present invention. In particular, Perets teaches arrangement of complete memory **banks** such that memory addresses are contiguous. According to Perets, a first memory **bank** is mapped as a negative offset with respect to the bottom address of a second memory **bank** such that the top address of the first memory bank has an offset of -1, and a bottom address of –(first **size**). The offset taught by Perets relates solely to the size of a memory **bank**. No teachings either in Frampton or Perets relates to the **filling** of memory downward, as claimed by claims 1-17.

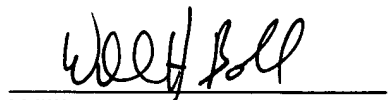
The Examiner cites col. 4, lines 4-16 of Feemster as allegedly curing yet another deficiency in the combination of Frampton and Perets, i.e., a first processor as not having access to a second mailbox. Nevertheless, even the combination of Frampton, Perets and Feemster if properly combined (which they are not with respect to claims 1-17) would still not teach a shared memory mailbox wherein a second mailbox portion addressably fills downward through to a **lowest** physical address, as claimed by claims 1-17.

Accordingly, for at least all the above reasons, claims 1-17 are patentable over the prior art of record. It is therefore respectfully requested that the rejection be withdrawn.

Conclusion

All objections and rejections having been addressed, it is respectfully submitted that the subject application is in condition for allowance and a Notice to that effect is earnestly solicited.

Respectfully submitted,



William H. Bollman
Reg. No. 36,457

Manelli Denison & Selter PLLC
2000 M Street, NW
Suite 700
Washington, DC 20036-3307
TEL. (202) 261-1020
FAX. (202) 887-0336